

Viterbi Decoder Netlist Core Short Description

Information about Release

Product	VITERBI-DECODER
Version	2.1
Release Date	2010.07
Ordering Code	ip-viterbi-decoder

Features

This IP Core is Viterbi Decoding algorithm and fully compatible with standards:

1. Digital Video Broadcasting (DVB-S, DVB-C, DVB-T);
2. CDMA2000 (3GPP2), 3GPP LTE;
3. IEEE 802.16 (WiMAX modems);
4. Intelsat IESS-308/309.

Deliverable

IP Core is content of:

- VQM or QXP or NGC Netlist Code for Target Device;
- Testbench for verification;
- Project examples for standard Evaluation Boards from Altera, Lattice and Xilinx.

IP Core structure

Figure 1 shows Viterbi Decoder IP Core structure.

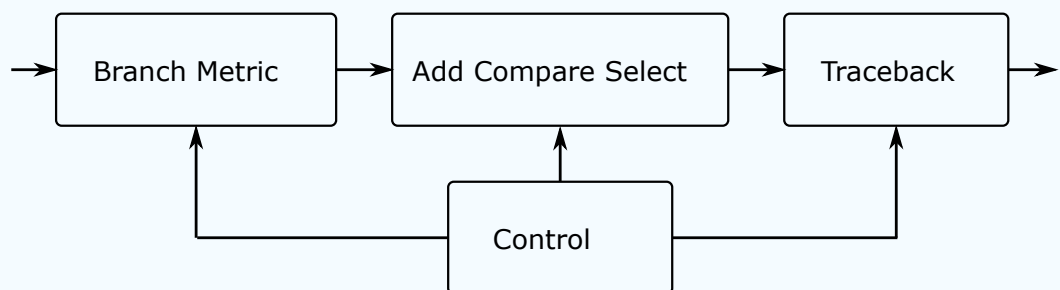


Figure 1. Structure of Viterbi Decoder IP Core

IP Core has classical structure and contents **Branch Metric**, **Add Compare Select** and **Traceback** blocks. For control and interface purpose there is **Control** block.

Port map

Figure 2 shows Viterbi Decoder graphical symbol, table 1 shows Viterbi Decoder port description.

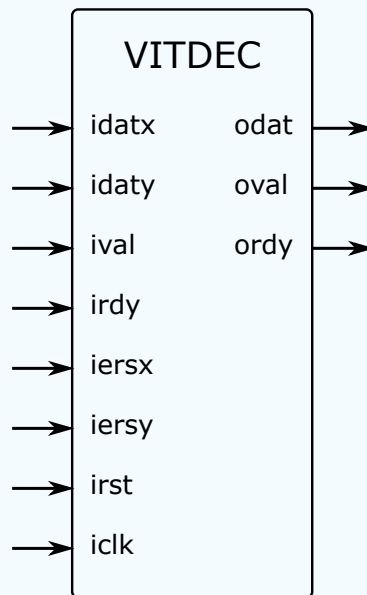


Figure 2. Viterbi Decoder Port Map

Table 1. Viterbi Decoder Port Map		
Port	Type	Description
idatx	input	input channel data
idaty	input	input channel data
ival	input	input data valid
irdy	input	ready to read output data
iersx	input	input data X pattern erase
iersy	input	input data Y pattern erase
irst	input	asynchronous reset
iclk	input	system clock
odat	output	output decoded data
oval	output	output data valid
ordy	output	ready for new input data

IP Core parameters

Table 2 shows parameters of Viterbi Decoder Netlist Core.

Table 2. Viterbi Decoder Parameters		
Parameter	Value	and Description
K	7	constraint length
POLY_X_Y	(171, 133) oct	generator polynome
W_IN	4	input data width
TRB	42	depth traceback

IP Core performance and resources

Table 3 shows Viterbi Decoder performance and resource results.

Table 3. Viterbi Decoder performance			
FPGA Type			
Resource	Speed grade, maximum frequency		
Altera Cyclone II EP2C35			
2,272 LEs 21,672 bits	-8, Fmax	-7, Fmax	-6, Fmax
	70.1 MHz	89.7 MHz	110.1 MHz
Xilinx Spartan-3A DSP XC3SD1800			
1,607 slices 21,672 bits	-4, Fmax	-5, Fmax	
	104.5 MHz	125.7 MHz	

IP Core timing diagrams

Figure 3 shows Viterbi decoder input timing diagrams. If the decoder becomes full because data is not being collected on the output side, it may deassert "ordy" until it can accept new data. The decoder only accepts data, if "ordy" is asserted.

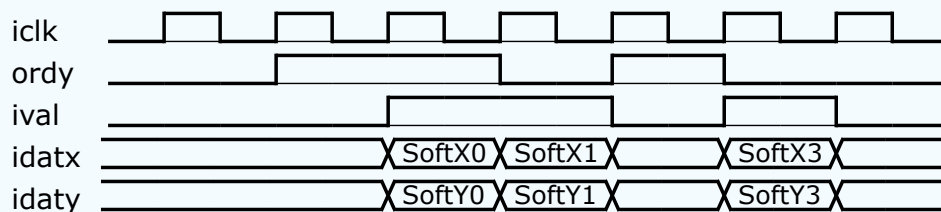


Figure 3. Viterbi Decoder input timing diagram

Figure 4 shows Viterbi decoder output timing diagrams. If "ival" is continuous, "oval" will be continuous. Empty cycles in the input stream will cause empty cycles in the output stream.

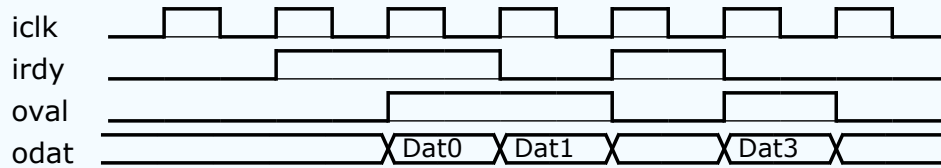


Figure 4. Viterbi Decoder output timing diagram

Figure 5 shows Viterbi decoder depuncturing timing diagram and shows "iersx", "iersy" for the pattern 110110 (puncturing rate 3/4). By changing the "iersx", "iersy" patterns you can implement virtually any depuncturing pattern you require.

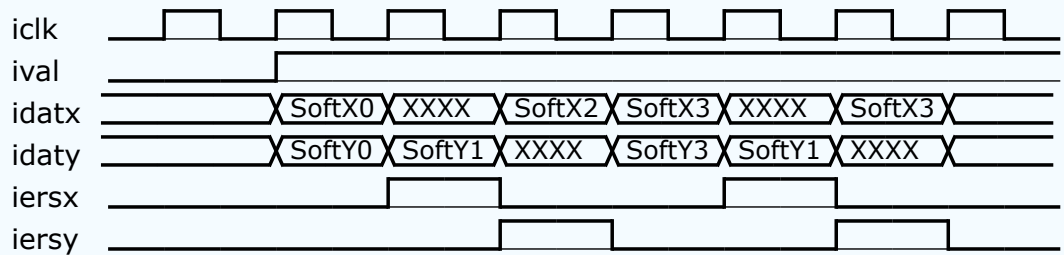


Figure 5. Viterbi Decoder depuncturing timing diagram

Updates and Technical Supports

Licensing terms include the delivery of a netlist for Viterbi Decoder that has a warranty certifying that it meets the written specification. The warranty period is usually 180 days.

Ordering Code

Ordering code of Viterbi Decoder IP Core is **ip-viterbi-decoder**.

Feedback

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